CBCS SCHEME

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15EC61

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With neat diagram, explain Canonical representation of Band – pass signal. **(10 Marks)**

b. Obtain Hilbert transform of the following :

i) $x(t) = \cos 2\pi f_c t + \sin 2\pi f_c t$ ii) $x(t) = e^{-j2\pi f_c t}$ iii) $x(t) = \delta(t)$. **(06 Marks)**

OR

2 a. Explain the complex representation of band pass signals and systems. **(07 Marks)**

b. Given the data stream 1011100101. Sketch the pulses for each of the following line code :

i) Unipolar RZ ii) Bipolar NRZ iii) Manchester code

iv) Polar quarternary (Natural code). **(04 Marks)**

c. Write a short note on HDB3 signaling. **(05 Marks)**

Module-2

3 a. Using the Gram – Schmidt Orthogonalization procedure, find a set of Orthonormal basis functions to represent the three signals $S_1(t)$, $S_2(t)$ and $S_3(t)$, shown in Fig. Q3(a). **(10 Marks)**

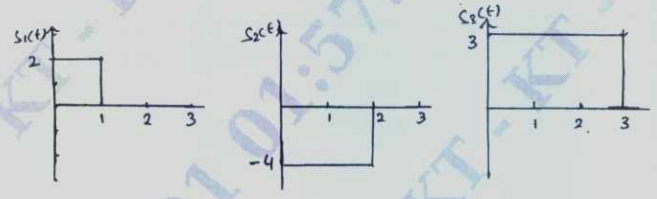

Fig. Q3(a)

b. Explain the matched filter receiver with mathematical expression. **(06 Marks)**

OR

4 a. Explain the Geometric representation of signals. Illustrate the geometric interpretation of signals for the case of 2 – dimensional signal space with 3 signals $S_1(3, 1)$, $S_2(1, 2)$, $S_3(2,3)$. **(07 Marks)**

b. Obtain the decision rule for ML decoding and explain Correlation receiver. **(09 Marks)**

Module-3

5 a. With a block diagram of QPSK transmitter and receiver, explain generation and demodulation of a QPSK wave. **(08 Marks)**

b. Obtain the expression for probability of error of BPSK. **(08 Marks)**

OR

6 a. With a neat diagram, explain the DPSK transmitter and receiver. **(07 Marks)**

b. Describe briefly M – ary QAM. Obtain the constellation of QAM for M = 4 and draw the signal space diagram. **(06 Marks)**

c. Draw the QPSK waveform for the sequence 0 1 1 0 1 0 0 0 showing in – phase and Quadrature components. **(03 Marks)**

Module-4

7 a. Explain the Nyquist criterion for distortion less base band binary transmission and obtain the ideal solution for zero ISI. **(08 Marks)**

b. What is Linear equalizer? With a neat diagram, explain the concept of equalization using a linear transversal filter. **(08 Marks)**

OR

8 a. With a neat block diagram, explain the digital PAM transmission through band limited base band channels and obtain the expression for ISI. **(06 Marks)**

b. What is Eye pattern? Explain with diagram, for binary and quaternary PAM and effect of ISI on eye opening. **(05 Marks)**

c. The binary sequence 1 1 1 0 1 0 0 1 0 0 0 1 1 0 1 is the input to the precoder. Obtain the precoded sequence, transmitted sequence , the received sequence and the decoded sequence. **(05 Marks)**

Module-5

9 a. With a neat block diagram, explain the concept of Frequency Hopped Spread Spectrum. **(07 Marks)**

b. Explain the effect of dispreading on a Narrow band interference with necessary diagram. **(04 Marks)**

c. Find the output sequence of the shift register shown in Fig. Q9(c). The initial state of the register is 1 1 1. Demonstrate the balance property and run property of a PN sequence. Also sketch the autocorrelation function. **(05 Marks)**

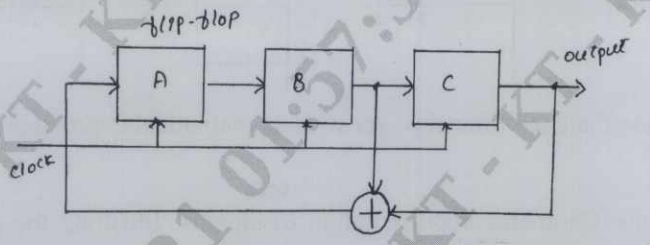

Fig. Q9(c)

OR

10 a. Explain the generation of Direct Sequence Spread Spectrum (DSSS) signal with relevant waveforms and spectrum. **(06 Marks)**

b. With a neat block diagram, explain the CDMA System based on IS – 95. **(07 Marks)**

c. Write a short note on Applications of Direct Sequence Spread Spectrum in CDMA. **(03 Marks)**

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CBCS SCHEME

USN [| | | | | | | | |] **15EC63**

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the nmos enhancement mode transistor operation for different values of V_{GS} and V_{DS}. **(06 Marks)**

b. Obtain the transfer characteristics of a CMOS inverter mark all the region, showing the status of PMOS and nmos transistor. **(10 Marks)**

OR

2 a. Explain the fabrication steps of CMOS P-well process with neat diagram, and write all the mask sequence. **(10 Marks)**

b. Distinguish between CMOS and bipolar technologies **(06 Marks)**

Module-2

3 a. With neat diagram, describe the design rules i) Transistor ii) wires iii) contact cut. **(08 Marks)**

b. Draw the Schematic and Mask Layout for the expression $Y = \overline{AB + CD}$. **(08 Marks)**

OR

4 a. Derive the expression for the Rise time and fall time for CMOS inverter. **(10 Marks)**

b. Two MOS inverters are cascaded to drive a capacitive load C_L = 14cg as shown in Fig Q4(b). Calculate the pair delays V_{in} to V_{out} in terms of τ.

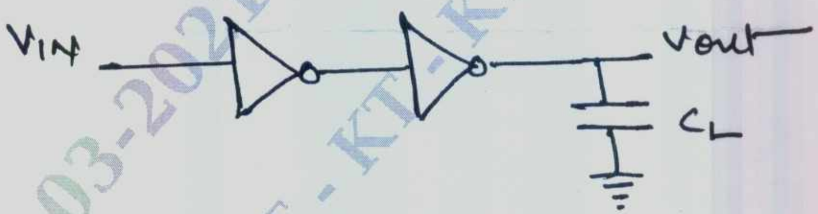

Fig Q4(b) **(06 Marks)**

Module-3

5 a. Why do we require scaling of MOS circuits? **(04 Marks)**

b. Find the scaling factors for the following :

i) Gate capacitance (C_g) ii) Saturation current (I_{ds})
iii) Gate capacitance per unit area (C_{ox}) iv) Carrier density in channel (Q_{ON})
v) Maximum frequency of operation (f_0) vi) Speed power product (P_T) **(12 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

6 a. Discuss the General considerations of the subsystem Design process. (06 Marks)
b. Explain a standard Adder element using nmos version of adder logic. (10 Marks)

Module-4

7 a. Explain the multiplexer/Data selections with layout. (10 Marks)
b. Explain parity Generator with stick diagram. (06 Marks)

OR

8 a. Briefly explain Architecture of FPGA. (10 Marks)
b. Explain Antifuse base FPGA. (06 Marks)

Module-5

9 a. Explain one transistor DRAM. (08 Marks)
b. Explain Three Transistors DRAM. (08 Marks)

OR

10 a. Explain objectives of Functional Testing. (06 Marks)
b. Define fault model, explain the
i) Stuck – at Faults
ii) Stuck – open and stuck – short Fault
iii) Stuck – open Fault (10 Marks)

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15EC64

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the following briefly;
   i) Data flow
   ii) Star topology
   iii) LAN
   iv) WAN **(08 Marks)**

b. With a neat diagram, explain TCP/IP protocol suite along with relevant diagram. **(08 Marks)**

OR

2 a. With a neat diagram, explain link layer addressing in detail. **(06 Marks)**

b. Explain character oriented framing and Bit oriented framing. **(05 Marks)**

c. Explain stop and wait protocol with FSM diagram. **(05 Marks)**

Module-2

3 a. With a neat diagram, explain standard Ethernet frame format and addressing. **(08 Marks)**

b. Differentiate pure ALOHA and slotted ALOHA protocol. **(04 Marks)**

c. A slotted ALOHA network transmits 200 bit frames using a shared channel with a 200kbps bandwidth. Find the throughput if the system produces:
   i) 1000 frames per second
   ii) 500 frames per second
   iii) 250 frames per second. **(04 Marks)**

OR

4 a. With a neat flow diagram, explain CSMA/CD random access protocol along with different persistence methods. **(08 Marks)**

b. In the standard Ethernet with the transmission rate of 10Mbps, the length of the medium is 2500m and the size of the frame is 512 bits. The propogation speed of a signal in a cable is 2×10^8m/s. Calculate propogation delay, transmission delay and efficiency. **(03 Marks)**

c. What are the goals of fast Ethernet and explain Augonegotiation. **(05 Marks)**

Module-3

5 a. Explain two types of packet switched networks. **(07 Marks)**

b. Explain Hubs, link layer switches, routers. **(06 Marks)**

c. Differentiate basic service set and extended service set. **(03 Marks)**

OR

6 a. Explain classful addressing in detail. **(05 Marks)**

b. An organization is granted a block of addresses with beginning address 14.24.74.0/24. The organization needs to have 3 sub blocks of addresses to use in three subnets: one subblock of 10 addresses, one subblock of 60 addresses, and one subblock of 120 addresses. Design the subblocks. **(07 Marks)**

c. What is Bluetooth? Explain two types of Bluetooth networks. **(04 Marks)**

Module-4

7 a. Explain IPV4 Datagram format and header fields with diagrams. **(08 Marks)**

b. Explain distance vector routing along with distance vector routing algorithm for a node. **(08 Marks)**

OR

8 a. Explain ICMPV4 message formats with diagram and explain error reporting messages. **(08 Marks)**

b. What is path vector routing and explain the same? **(06 Marks)**

c. In an IPV4 packet, the value of HLEN is 5, and the value of the total length field is OX0028. How many bytes of data are being carried by this packet? **(02 Marks)**

Module-5

9 a. Explain connectionless and connection oriented protocols in transport layer. **(08 Marks)**

b. Explain Goback N protocol along with sliding window diagrams. **(08 Marks)**

OR

10 a. Explain TCP segment format along different fields. **(08 Marks)**

b. With a neat diagram, explain state transition diagram of TCP. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Jan./Feb.2021
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Construct with neat diagram, the simple design methodology and describe functions. **(08 Marks)**

b. Compute a design methodology for Hardware or Software codesign used in embedded system. **(08 Marks)**

OR

2 a. Construct and write verilog code for the Burglar alaram to be a priority Encoder, with zone 1 having highest priority, down to zone 8 having lowest priority, using truth table. **(08 Marks)**

b. Develop Data Path and Verilog model of the complex multiplier. **(08 Marks)**

Module-2

3 a. Design 64K*8 bit composite memory using four 16K*8 bit components. **(08 Marks)**

b. Describe all types of ROM. **(08 Marks)**

OR

4 a. Explain ECC code and and compute whether there is an error in the ECC word 000111000100, if so, correct it. **(08 Marks)**

b. Design and develop a verilog model of 7-segment decoder with blanking input using ROM. **(08 Marks)**

Module-3

5 a. With neat diagram, describe the Application Specific Integrated Circuits (ASICS). **(06 Marks)**

b. Compute design of Programmable Array Logic (PAL). **(10 Marks)**

OR

6 a. Compute the design of Field Programmable Gate Arrays (FPGA). **(10 Marks)**

b. Design a priority encoder has 16 inputs I[0:15]; four-bit encoded output Z[3:0]; & a valid output is 1, when any input I[0] has the highest priority and I[15]. The lowest priority. Express in verilog. **(06 Marks)**

Module-4

7 a. Describe all parallel buses used in digital circuits I/O devices. **(08 Marks)**

b. Describe all serial interface standard for connecting I/O devices. **(08 Marks)**

OR

8 a. Describe all types of interrupts used in I/O interfacing. **(08 Marks)**

b. Design an I/P controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value change. The controller is the only interrupt source in the system and design a verilog model of the input controller. **(08 Marks)**

Module-5

9	a.	Describe area and time optimization used in design optimization.	(08 Marks)
	b.	Describe scan design and boundary system.	(08 Marks)

OR

10	a.	Describe Built-In Self Test (BIST) using in Design methodology.	(08 Marks)
	b.	Describe physical Design using in design flow.	(08 Marks)

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